



Latchup

By Steven H. Voldman

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Interest in latchup is being renewed with the evolution of complimentary metal-oxide semiconductor (CMOS) technology, metal-oxide-semiconductor field-effect transistor (MOSFET) scaling, and high-level system-on-chip (SOC) integration.

Clear methodologies that grant protection from latchup, with insight into the physics, technology and circuit issues involved, are in increasing demand.

This book describes CMOS and BiCMOS semiconductor technology and their sensitivity to present day latchup phenomena, from basic over-voltage and over-current conditions, single event latchup (SEL) and cable discharge events (CDE), to latchup domino phenomena. It contains chapters focusing on bipolar physics, latchup theory, latchup and guard ring characterization structures, characterization testing, product level test systems, product level testing and experimental results. Discussions on state-of-the-art semiconductor processes, design layout, and circuit level and system level latchup solutions are also included, as well as:

- latchup semiconductor process solutions for both CMOS to BiCMOS, such as shallow trench, deep trench, retrograde wells, connecting implants, sub-collectors, heavily-doped buried layers, and buried grids – from single- to triple-well CMOS;
- practical latchup design methods, automated and bench-level latchup testing methods and techniques, latchup theory of logarithm resistance space, generalized alpha (α) space, beta (β) space, new latchup design methods—connecting the theoretical to the practical analysis, and;
- examples of latchup computer aided design (CAD) methodologies, from design rule checking (DRC) and logical-to-physical design, to new latchup CAD methodologies that address latchup for internal and external latchup on a local as well as global design level.

Latchup acts as a companion text to the author's series of books on ESD (electrostatic discharge) protection, serving as an invaluable reference for the professional semiconductor chip and system-level ESD engineer. Semiconductor device, process and circuit designers, and quality, reliability and failure analysis engineers will find it informative on the issues that confront modern CMOS

technology. Practitioners in the automotive and aerospace industries will also find it useful. In addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, computer aided design and design integration.

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Editorial Review

From the Back Cover

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About the Author

Steven H. Voldman is an IEEE Fellow for 'Contributions in ESD Protection in CMOS, Silicon on Insulator and Silicon Germanium Technology'. He has a B.S. engineering science from University of Buffalo (1979), a first M.S. EE (1981) from Massachusetts Institute of Technology (MIT), a second EE degree (engineering degree) from MIT, a M.S. in engineering physics (1986) and a Ph.D. EE (1991) from University of Vermont under IBM's Resident Study Fellow Program.

Since 1984, Voldman has provided experimental research, invention, chip design integration, circuit design, customer support and strategic planning for ESD and latchup. His latchup and ESD work consist of pioneering work on advanced CMOS and BiCMOS semiconductor processing, and presently he is working on RF CMOS, RF BiCMOS silicon germanium (SiGe) technology, image processing and high-voltage smart

power technology.

Dr Voldman has written over 150 technical papers between 1982 and 2007. He is a recipient of over 160 issued US patents and 80 US patents are pending, in the area of ESD and CMOS latchup, Dr Voldman is an author of the John Wiley & Sons ESD book series - the first book, ESD: Physics and Devices; the second book, ESD: Circuits and Devices; and the third book, ESD: RF Technology and Circuits - as well as a contributor to the book, Silicon Germanium: Technology, Modeling and Design. Dr. Voldman was chairman of the SEMATECHESD Working Group from 1995 to 2000, to establish a national strategy for ESD in the United States; this group initiated ESD technology benchmarking strategy, test structures and commercial test system strategy. Dr Voldman was also part of the SEMATECH vertical modulated well PTAB in 1992 that focused on MeV implantation of latchup. He is a member of the ESD Association Board of Directors, ESDA Education Committee, as well ESD Standards Chairman for Transmission Line Pulse (TLP) and Very Fast TLP (VF-LP) testing committee. He has served on various Symposia internationally from technical program committee to tutorials on ESD and latchup - EOS/ESD Symposium, International Reliability Physics (IRPS), Taiwan ESSD Symposium (T-ESDC), International Conference on Electromagnetic Compatibility (ICEMAC), International Physical and Failure Analysis (IPFA) Symposium and Bipolar/BiCMOS Circuit Technology Meeting (BCTM).

Steve Voldman Initiated the 'ESD on Campus' program to bring ESD lectures and interaction to university faculty and students internationally and has provided lectures in the United States, Europe, Taiwan, Singapore, Malaysia, Philippines, China and Thailand. Dr. Voldman received the ESD Association Outstanding Contribution Award in 2007.

Users Review

From reader reviews:

Jamie Brewer:

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